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METHOD FOR CHECKING THE REFRESH FUNCTION OF AN INFORMATION MEMORY

Background of the Invention:

Field of the Invention:

The present invention relates to a method for checking the refresh function of a memory for storing information.

Particular types of memories for storing information, particularly those with memory cells of the dynamic type, require "refresh operations" within prescribed periods of time. These operations involve the information stored in a memory cell briefly being read out and written back to the cell in unchanged form. Without such refresh operations, the memory cells would lose the information stored in them within a very short time. The reason for such loss can be found in the construction of the memory cells: the information stored in them is being reduced constantly by unavoidable leakage currents, which means that, in the absence of the refresh operations, it can no longer be recognized as the original information upon reading after a certain time. This is general knowledge in relevant technical circles.

For such reasons, many of these memories, today, have a refresh device that performs the refresh operation automatically or upon request based upon prescribed criteria. Because such refresh operations require a finite time to be executed, there are various ways of connecting the sequence of these refresh operations to the normal mode of the memory in a suitable manner over time. Like all the other components of such memories, the operation of these refresh devices also needs to be tested. By way of example, German Published, Non-Prosecuted Patent Application DE 100 04 958 A1, corresponding to United States Patent Publication 2001/027,541 A1 to Richter et al., discloses a method for testing the refresh device in a memory for storing information. A drawback of this method is that, when an error occurs during testing, it is not known if one or more components of the tested refresh device is/are faulty.

Summary of the Invention:

It is accordingly an object of the invention to provide a method for checking the refresh function of an information memory that overcomes the hereinafore-mentioned disadvantages of the heretofore-known devices and methods of this general type and that permits more accurate inferences about the causes of malfunctions that arise.

With the foregoing and other objects in view, there is provided, in accordance with the invention, a method for checking the refresh function of a memory having a refresh device, including determining if refresh request pulses are being produced on the memory and at what intervals of time the refresh request pulses are being produced on the memory, supplying a control unit of the memory with refresh test pulses produced outside the memory instead of supplying the control unit with the refresh request pulses, and checking the refresh device of the memory utilizing the refresh test pulses.

In accordance with another mode of the invention, the control unit controls the checking of the refresh device.

In accordance with a further feature of the invention, the refresh test pulses and the refresh request pulses are supplied to a multiplex device. Preferably, the refresh test pulses and the refresh request pulses are supplied to the control unit through a multiplex device.

In accordance with an added feature of the invention, a multiplex device is connected to the control unit and the refresh test pulses and the refresh request pulses are supplied to the control unit through the multiplex device.

In accordance with a concomitant feature of the invention, the multiplex device is controlled with a test signal.

Other features that are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in a method for checking the refresh function of an information memory, it is, nevertheless, not intended to be limited to the details shown because various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof, will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawing:

The figure is a block and schematic circuit diagram of individual elements of a memory for storing information according to the invention and a flow of signals significant to the invention.

Description of the Preferred Embodiments:

Referring now to the single figure of the drawing, elements of significance to the present invention that are part of the memory to be checked are shown within a dash-dot line. These elements are a (normally freely cycling) internal oscillator Osc, a counter Cnt, a multiplex device MUX, a control unit CTRL, and a memory cell array MEM containing the memory cells to be refreshed and containing a refresh device. The refresh device can be of the type presented in the aforementioned German Published, Non-Prosecuted Patent Application DE 100 04 958 A1, corresponding to United States Patent Publication 2001/027,541 A1 to Richter et al., for example. A pad pd on the memory is also indicated. With the exceptions of the pad pd and the multiplex device MUX, all the elements shown are also already present in a memory that cannot be tested using the inventive method. This means that only very little involvement and, in particular, very little additional chip area are required in order to equip a conventional memory such that its refresh function can be tested using the method according to the invention. Outside of the memory, there are also an external, freely cycling oscillator Osc_{ext} and an external counter Cnt_{ext}, which are used for carrying out the inventive method. Both can be part of a test machine, for example. There are also known (ordinary) instances of application of memories in which an external oscillator is also already available for the normal mode of the memory. Such

an oscillator can, then, naturally be used as the aforementioned external, freely cycling oscillator Osc_{ext}.

The inventive method, now, proceeds as set forth in the following text.

In a first step, it is ascertained whether or not refresh request pulses Ref are being produced on the memory, which can be an integrated semiconductor memory of the DRAM type, for example. If the memory is intact, these refresh request pulses Ref are used in the normal mode to trigger a refresh operation. In practice, there are great demands on these refresh request pulses Ref: first, they need to observe a prescribed interval of time from one another. If this interval is exceeded, the guaranteed "retention time" (= minimum period of time, guaranteed by the memory manufacturer, within which stored information will not "be lost") is exceeded, i.e., necessary refresh operations do not take place in time or in full, which can result in data losses. Secondly, such refresh request pulses Ref should not appear all too often either because refresh operations would, then, be performed more often than is technically necessary, resulting in unnecessarily increased power consumption. Consequently, the first step ascertains not just if the refresh request pulses Ref actually appear, but also at what interval of time from one another they occur. Thus, if this test ascertains that the

refresh request pulses Ref are actually appearing and also at the right time, then there is already a firm first partial result that states that a first prerequisite for the performance of regular refresh operations in the normal mode of the information memory is satisfied.

The drawing shows a pad pd on the memory that can be used to perform the afore-mentioned test on the refresh request pulses Ref. This pad pd can also be connected to a pin on a chip that contains the memory, which means that the refresh request pulses Ref are available on the pin (outside of the chip) and can, thus, also be picked off. If test needles or test electrodes of sufficiently small dimensions are available, the afore-mentioned ascertainment can also be performed directly on an appropriate interconnect in the memory. In such a case, the pad pd becomes unnecessary.

In the normal mode of a memory, the usual refresh operation is performed such that a circuit that can be referred to generally as a control unit CTRL is supplied with the refresh request pulses Ref. The control unit CTRL (which provides important control signals and/or data signals for operating the memory cell array MEM together with its refresh device and supplies the signals to the memory cell array MEM) modifies a portion of these signals when a refresh request pulse Ref is currently present such that a single cycle does not just

involve a memory cell being read (or written to, depending on the request) in regular fashion, but, rather, memory cells (usually all the memory cells along one word line) are also refreshed. The latter generally occurs within the cycle before reading or writing.

In the case of the inventive method, on the other hand, the control unit CTRL is supplied with refresh test pulses RTest instead of being supplied with the refresh request pulses Ref, the refresh test pulses RTest being, in turn, supplied to the information memory externally, for example, using an external, freely cycling oscillator Osc_{ext} and an external counter Cnt_{ext} connected thereto. This means that precisely a desired number of refresh test pulses RTest can be set per unit time, and, hence, their interval of time from one another; during testing, there is no dependence on the number of refresh request pulses Ref per unit time that is implemented on the memory itself.

It is possible to change over between supply of the refresh request pulses Ref and supply of the refresh test pulses RTest using a multiplex device MUX. This can be in a form such that, in the memory's normal mode, it has an "idle" setting in which the refresh request pulses Ref are connected through to the control unit CTRL, while in the test mode a test signal Test supplied to the memory externally is applied with a prescribed

signal level to the multiplex device MUX to control it as appropriate, i.e., to change it over. The test signal Test can also be a given an electrical potential that is already provided as such on the memory independently of a test mode and can be applied to the multiplex device MUX during testing.

While the refresh test pulses RTest are being supplied to the control unit CTRL, the refresh device's operation is checked, under the control of the control unit CTRL. It is advantageous in this case if this check is carried out as disclosed in the aforementioned German Published, Non-Prosecuted Patent Application DE 100 04 958 A1, corresponding to United States Patent Publication 2001/027,541 A1 to Richter et al.

The inventive method, thus, provides a simple way -- with almost no involvement -- of establishing, an from additional area on the memory, whether or not the memory's individual components involved in the appearance of refresh operations (that is to say, in the present case: memory-internal oscillator Osc with downstream counter Cnt, control unit CTRL, and the refresh device, itself) are operating correctly.